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NON-LITHOGRAPHIC SHRINK TECHNIQUES FOR IMPROVING LINE EDGE ROUGHNESS AND USING IMPERFECT (BUT SIMPLER) BARCs

by

Gilles Amblard, Bhanwar Singh,
Khoi A. Phan and Ramkumar Subramanian

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Himanshu S. Amin

TITLE: NON-LITHOGRAPHIC SHRINK TECHNIQUES FOR IMPROVING LINE EDGE ROUGHNESS AND USING IMPERFECT (BUT SIMPLER) BARCs

TECHNICAL FIELD

The present invention relates generally to photolithographic systems and methods, and more particularly to systems and methodologies that facilitate mitigating line-edge roughness and/or standing waves on pattern profiles during formation of an integrated circuit.

BACKGROUND OF THE INVENTION

As semiconductor trends continue toward decreased size and increased packaging density, every aspect of semiconductor fabrication processes is scrutinized in an attempt to maximize efficiency in semiconductor fabrication and throughput. Many factors contribute to fabrication of a semiconductor. For example, at least one photolithographic process can be used during fabrication of a semiconductor. This particular factor in the fabrication process is highly scrutinized by the semiconductor industry in order to improve packaging density and precision in semiconductor structure.

Lithography is a process in semiconductor fabrication that generally relates to transfer of patterns between media. More specifically, lithography refers to transfer of patterns onto a thin film that has been deposited onto a substrate. The transferred patterns then act as a blueprint for desired circuit components. Typically, various patterns are transferred to a photoresist (*e.g.*, radiation-sensitive film), which overlies the thin film on the substrate during an imaging process described as "exposure" of the photoresist layer. During exposure, the photoresist is subjected to an illumination source (*e.g.* UV-light, electron beam, X-ray), which passes through a pattern template, or reticle, to print the desired pattern in the photoresist. Upon exposure to the illumination source, radiation-sensitive qualities of the photoresist permit a chemical transformation in

exposed areas of the photoresist, which in turn alters the solubility of the photoresist in exposed areas relative to that of unexposed areas. When a particular solvent developer is applied, exposed areas of the photoresist are dissolved and removed, resulting in a three-dimensional pattern in the photoresist layer. This pattern is at least a portion of the semiconductor device that contributes to final function and structure of the device, or wafer.

Techniques, equipment and monitoring systems have concentrated on preventing and/or decreasing defect occurrence within lithography processes. For example, aspects of resist processes that are typically monitored can comprise: whether the correct mask has been used; whether resist film qualities are acceptable (*e.g.*, whether resist is free from contamination, scratches, bubbles, striations, ...); whether image quality is adequate (*e.g.*, good edge definition, line-width uniformity, and/or indications of bridging); whether critical dimensions are within specified tolerances; whether defect types and densities are recorded; and/or whether registration is within specified limits; *etc.* Such defect inspection task(s) have progressed into automated system(s) based on both automatic image processing and electrical signal processing.

Photoresist integrity must be maintained throughout the lithography process because any flaw or structural defect present on a patterned photoresist can be indelibly transferred to underlying layers during asubsequent etch process(es) wherein the photoresist is employed. One example of an undesirable structural defect is line-edge roughness (LER). LER refers to variations on sidewalls of features, which can result from variations of LER in the patterned photoresist. Many factors can contribute to LER in the photoresist, such as LER on chrome patterns residing on the reticle, image contrast in a system that generates the photoresist pattern, a plasma etch process that can be used to pattern the photoresist, inherent properties and/or weaknesses of the photoresist materials, and/or the photoresist processing method. Additionally, LER appearing in fabricated structures can result from damage to the patterned photoresist during an etch process. Furthermore, the smaller the wavelength employed to expose a photoresist, the greater the deleterious effects of LER.

Current methods of pattern line formation typically produce LER as an undesirable side effect. As lithographic techniques are pushed to their limits, smaller and smaller critical dimensions (CDs) are desired to maximize chip

performance. Thus, chip manufacture is governed largely by wafer CD, which is defined as the smallest allowable width of, or space between, lines of circuitry in a semiconductor device. As methods of wafer manufacture are improved, wafer CD is decreased, which in turn requires finer and finer line edges to be produced. Line edges having a roughness that was acceptable just a year ago can detrimentally affect the performance of a chip exhibiting today's critical dimension standards.

Another example of undesirable structural defects are standing waves. Standing waves can occur when imperfections exist in a bottom anti-reflective layer (BARC). During an etch step performed, for example, on a resist layer that overlies a BARC layer, standing waves extant within the resist layer can be expressed. Such exposed standing waves can cause an etched surface (*e.g.*, a sidewall) to display undulate topography, thus contributing to LER. Current methods of mitigating standing waves in a resist layer require the utilization of "perfect" BARCs, which are expensive and highly complicated with regard to implementation thereof during a photolithographic process(es).

SUMMARY OF THE INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an extensive overview of the invention. It is not intended to identify key/critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts of the invention in a simplified form as a prelude to the more detailed description that is presented later.

The present invention provides for systems and methods that facilitate mitigation of line-edge roughness (LER) and/or standing waves on pattern lines formed in a photoresist during integrated circuit (IC) manufacture. More specifically, the systems and methods of the invention can mitigate LER and/or standing waves that can result from the utilization of imperfect bottom anti-reflective coatings (BARCs) during wafer manufacture, while maintaining critical dimension (CD) within a target tolerance.

An aspect of the present invention provides for techniques that can be employed to mitigate LER and/or standing wave expression on pattern lines in a

resist overlying a potentially imperfect BARC. For example, a monitoring component can determine whether LER and/or standing waves exist on pattern lines in a resist. If it is determined that LER and/or standing waves are present, a non-lithographic shrink technique can be performed on the pattern line(s) to mitigate LER. In order to prevent departure from a target CD between pattern lines, the shrink technique can be employed utilizing a minimum functional temperature, at which undesirable topography is mitigated while target CD is retained.

According to one aspect, the non-lithographic shrink technique can be a thermal flow technique, whereby a resist is heated to a predetermined minimum temperature, such as, for example, the glass transition temperature of the resist, so that the resist begins to exhibit fluid properties and begins to flow. By causing the resist to just enter a liquid phase, LER is mitigated because the solid physical state of the photoresist is compromised. The temperature to which the resist is heated can be high enough to mitigate LER and/or standing wave expression but low enough to avoid an increase in CD. In this manner, the invention advantageously mitigates LER while maintaining CD within a desired tolerance.

According to another aspect, the invention can employ a Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS™) technique. For example, contact holes and/or gate channels can be shrunk to facilitate achieving Deep UV and/or Extreme UV dimensions. According to yet another aspect of the invention, a Shrink Assist Film for Enhanced Resolution (SAFIER) technique can be employed to facilitate a controlled shrink of, for example, a contact opening or a gate channel. This technique is capable of shrinking a contact opening down to about 50nm.

To the accomplishment of the foregoing and related ends, certain illustrative aspects of the invention are described herein in connection with the following description and the annexed drawings. These aspects are indicative, however, of but a few of the various ways in which the principles of the invention can be employed and the present invention is intended to comprise all such aspects and their equivalents. Other advantages and novel features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an illustration of a system in accordance with an aspect of the present invention.

Figure 2 is an illustration of a system in accordance with an aspect of the present invention comprising a processor and a memory.

Figure 3 is an illustration of a system in accordance with the present invention wherein a processor comprises an artificial intelligence component.

Figure 4a is a cross-sectional illustration of a wafer with pattern lines exhibiting line-edge roughness (LER).

Figure 4b is a top-down illustration of a wafer with pattern lines exhibiting LER.

Figure 5a is an illustration of a system in accordance with an aspect of the present invention wherein a non-lithographic shrink technique is applied to mitigate LER.

Figure 5b is a top-down illustration of a wafer with pattern lines exhibiting LER presented to permit comparison with the cross-sectional view of the wafer of 5a.

Figure 6a is an illustration of a wafer after application of a non-lithographic shrink technique.

Figure 6b is a top-down illustration of a wafer with pattern lines where LER has been mitigated and critical dimension (CD) has been retained.

Figure 7a is a perspective cross-sectional illustration of pattern lines on a photoresist exhibiting LER in three planes.

Figure 7b is a perspective cross-sectional illustration of pattern lines on a photoresist wherein LER has been mitigated and CD has been retained.

Figure 7c is a top-down illustration of pattern lines exhibiting LER, presented to permit comparison with the perspective view of the pattern lines of 7a.

Figure 7d is a top-down illustration of a pattern lines wherein LER has been mitigated, presented to permit comparison with the perspective view of the pattern lines of 7b.

Figure 8a is a cross-sectional illustration of a wafer with contact holes wherein standing waves have been exposed.

Figure 8b is a cross-sectional illustration of a wafer with contact holes wherein standing wave expression has been mitigated.

Figure 8c is a top-down illustration of a wafer with contact holes wherein standing waves have been exposed.

Figure 8d is a top-down illustration of a wafer with contact holes wherein standing wave expression has been mitigated.

Figure 9 illustrates a perspective view of a grid-mapped wafer according to one or more aspects of the present invention.

Figure 10 illustrates plots of measurements taken at grid-mapped locations on a wafer in accordance with one or more aspects of the present invention.

Figure 11 illustrates a table containing entries corresponding to measurements taken at respective grid-mapped locations on a wafer in accordance with one or more aspects of the present invention.

Figure 12 is an illustration of a flow diagram of a methodology in accordance with an aspect of the present invention.

Figure 13 is an illustration of a flow diagram of a methodology in accordance with an aspect of the present invention.

Figure 14 is an illustration of a flow diagram of a methodology in accordance with an aspect of the present invention.

Figure 15 is an illustration of an exemplary computing system and/or environment in connection with facilitating employment of the subject invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will now be described with reference to the drawings, wherein like reference numerals are used to refer to like elements throughout. The present invention will be described with reference to systems and methods for mitigating line-edge roughness (LER) and/or standing wave expression during pattern line formation in a photoresist while maintaining critical dimension (CD) within a target tolerance. It should be understood that the description of these exemplary aspects are merely illustrative and that they should not be taken in a limiting sense.

The term "component" refers to a computer-related entity, either hardware, a combination of hardware and software, software, or software in execution. For

example, a component can be a process running on a processor, a processor, an object, an executable, a thread of execution, a program and a computer. By way of illustration, both an application running on a server and the server can be components. A component can reside in one physical location (*e.g.*, in one computer) and/or can be distributed between two or more cooperating locations (*e.g.*, parallel processing computer, computer network).

It is to be appreciated that various aspects of the present invention can employ technologies associated with facilitating unconstrained optimization and/or minimization of error costs. Thus, non-linear training systems/methodologies (*e.g.*, back propagation, Bayesian, fuzzy sets, non-linear regression, or other neural networking paradigms including mixture of experts, cerebella model arithmetic computer (CMACS), radial basis functions, directed search networks, and function link networks) can be employed.

It is further to be appreciated that any and all discussion herein of "standing wave(s)," "standing wave expression," "standing wave exposure," *etc.*, is intended to refer to the phenomenon of standing wave(s) within a photoresist. Additionally, the above-mentioned phrases can refer to edge roughness created when a standing wave is exposed during etching, such that LER results *via* the "expression" of a standing wave that was previously completely within the photoresist (*e.g.*, "unexpressed"). In this regard, the phrase "LER" can be mutually inclusive of "standing wave expression," *etc.*, and/or "LER" can refer to LER caused by means unassociated with standing wave(s).

Figure 1 is an illustration of an LER and/or standing wave mitigation system 100 according to an aspect of the present invention. The LER and/or standing wave mitigation system 100 comprises a non-lithographic shrink component 102 that is operatively coupled to a monitoring component 104. According to this aspect of the invention, resist lines are formed in a photoresist *via* conventional methods. The monitoring component 104 can analyze and determine whether threshold LER exists on the pattern lines, and/or whether CD is within a target tolerance. The monitoring component 104 can employ scatterometry techniques to perform the preceding analysis.

It is to be appreciated that the monitoring component 104 can be, for example, a scatterometry component. The present invention contemplates any suitable scatterometry component and/or system, and such systems are intended to

fall within the scope of the hereto-appended claims. It is further to be appreciated that the monitoring component 104 utilized by the present invention can be, for example, a Scanning Electron Microscope (SEM), a Critical Dimension Scanning Electron Microscope (CD-SEM), a Field Effect Scanning Electron Microscope (FESEM), an In-Lens FESEM, or a Semi-In-Lens FESEM, depending on the desired magnification and precision. For example, FESEM permits greater levels of magnification and resolution at high or low energy levels by rastering a narrower electron beam over the sample area. FESEM thus permits quality resolution at approximately 1.5nm. Because FESEM can produce high-quality images at a wide range of accelerating voltages (typically 0.5kV to 30kV), it is able to do so without inducing extensive electrical charge in the sample. Furthermore, conventional SEM cannot accurately image an insulating material unless the material is first coated with an electrically conductive material. FESEM mitigates the need for the deposit of an electrically conductive coating prior to scanning. According to another example, the monitoring component 104 of the present invention can be In-Lens FESEM, which is capable 0.5nm resolution at an accelerating voltage of 30kV, or any other suitable type of scanner, such as Transmission Electron Microscopy (TEM), Atomic Force Microscopy (AFM), Scanning Probe Microscopy (SPM), *etc.*

It is further to be appreciated that information gathered by the monitoring component 104 can be utilized for generating feedback and/or feed-forward data that can facilitate maintaining critical dimensions that are within acceptable tolerances. The LER and/or standing wave mitigation system 100 can additionally employ such data to control components and/or operating parameters associated therewith. For instance, feedback/feed-forward information can be generated from sequence analysis to maintain, increase and/or decrease a rate at which fabrication processes (*e.g.,* thermal reflow, etching, ...) progress. Additionally, one or a plurality of sensors can be associated with the LER and/or standing wave mitigation system to permit data to be gathered regarding the state of the wafer (*e.g.*, temperature, density, viscosity, material composition, and/or any other suitable information related to the condition of the wafer).

Upon determining that a threshold amount of LER and/or standing wave expression is present, the system 100 can mitigate LER and/or standing wave expression by employing the non-lithographic shrink component 102. To avoid

any increase in CD during the shrink technique, the system 100 can heat the resist to a minimum temperature at which LER and/or standing wave expression can be mitigated. For example, the temperature to which the resist is heated can be high enough to reduce LER, but low enough to preclude any increase in CD. Additionally, duration of exposure to the minimum reaction temperature can be accounted for in order to ensure that CD remains within a target tolerance. Thus, the instant invention can advantageously mitigate LER and/or standing wave formations associated with pattern line formation in a photoresist while preserving a desired CD.

According to an aspect of the invention, the non-lithographic shrink component 102 can be a thermal flow component that is capable of heating a resist (not shown) in which pattern lines have been formed to a temperature at which the resist will begin to flow. Such a temperature is often referred to as the "glass transition temperature" of the resist, which describes a temperature near the resist softening point and at which the resist begins to flow. By causing the resist to begin to flow, jagged edges associated with LER and/or standing waves can be smoothed (*e.g.*, mitigated). Additionally, the non-lithographic shrink component 102 can be a Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS™) component. For example, contact holes and/or gate channels can be manipulated to facilitate achieving Deep UV and/or Extreme UV dimensions. According to another example, the non-lithographic shrink component 102 can be a Shrink Assist Film for Enhanced Resolution (SAFIER) component that can facilitate a controlled shrink of, for example, a contact opening or a gate channel. *Via* employing a SAFIER technique, a SAFIER component can shrink a contact opening down to about 50nm.

Figure 2 illustrates an LER and/or standing wave mitigation system 200 in accordance with an aspect of the present invention. The LER and/or standing wave mitigation system 200 comprises a non-lithographic shrink component 202 that is operably coupled to a monitoring component 204. According to this aspect, the monitoring component 204 is further operably coupled to a processor 206, which is in turn operably coupled to a memory 208. It is to be understood that a that the processor 206 can be a processor dedicated to determining whether LER exists, a processor used to control one or more of the components of the present system(s), or, alternatively, a processor that is both used to determine

whether LER exists and to control one or more of the components of the LER mitigation system.

The memory component 208 can be employed to retain control programs, semiconductor fabrication data, *etc.* Furthermore, the memory 208 can be either volatile memory or nonvolatile memory, or can comprise both volatile and nonvolatile memory. By way of illustration, and not limitation, nonvolatile memory can comprise read only memory (ROM), programmable ROM (PROM), electrically programmable ROM (EPROM), electrically erasable ROM (EEPROM), or flash memory. Volatile memory can comprise random access memory (RAM), which acts as external cache memory. By way of illustration and not limitation, RAM is available in many forms such as synchronous RAM (SRAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), double data rate SDRAM (DDR SDRAM), enhanced SDRAM (ESDRAM), Synchlink DRAM (SLDRAM), and direct Rambus RAM (DRRAM). The memory 208 of the present systems and methods is intended to comprise, without being limited to, these and any other suitable types of memory.

Figure 3 is an illustration of an LER and/or standing wave mitigation system 300 in accordance with an aspect of the present invention. The LER and/or standing wave mitigation system 300 can employ various inference schemes and/or techniques in connection with mitigating LER and/or standing wave expression and retaining a target CD. As used herein, the term "inference" refers generally to the process of reasoning about or inferring states of the system, environment, and/or user from a set of observations as captured *via* events and/or data. Inference can be employed to identify a specific context or action, or can generate a probability distribution over states, for example. The inference can be probabilistic - that is, the computation of a probability distribution over states of interest based on a consideration of data and events. Inference can also refer to techniques employed for composing higher-level events from a set of events and/or data. Such inference results in the construction of new events or actions from a set of observed events and/or stored event data, whether or not the events are correlated in close temporal proximity, and whether the events and data come from one or several event and data sources. Various classification schemes and/or systems (*e.g.*, support vector machines, neural networks, expert systems, Bayesian belief networks, fuzzy logic, data fusion engines…) can be employed in

connection with performing automatic and/or inferred action in connection with the subject invention.

Still referring to Figure 3, the LER and/or standing wave mitigation system 300 comprises a non-lithographic shrink component 302 that is operably coupled to a monitoring component 304. A processor 306 is operably coupled to both a memory 308 and the monitoring component 304. According to this aspect of the invention, the processor 306 is associated with an artificial intelligence (AI) component 310 that can make inferences regarding system operation. For example, the AI component 310 can determine an optimal duration for employing the non-lithographic shrink component 302. Additionally, the AI component can make inferences regarding an optimal temperature at which to expose the resist lines to facilitate mitigating LER and/or standing wave expression while avoiding any undesired increase in CD. According to another example, the AI component 310 can make inferences regarding whether target CD has been retained. These examples are given by way of illustration only and are not in any way intended to limit the scope of the present invention or the number of, or manner in which the AI component makes, inferences.

Figure 4a is a cross-sectional illustration of a wafer 400 with extant resist lines exhibiting LER and/or standing wave expression. The wafer 400 comprises a silicon or polysilicon substrate 402, at least one layer of dielectric material 404 overlying the substrate 402, and a bottom anti-reflective coating, or BARC layer 406, which is interposed between the dielectric layer(s) 404 and a photoresist layer 408. The at least one dielectric layer can be, for example, a silicon carbonitride layer (SiCN), a silicon oxycarbide layer (SiOC:H), a silicon dioxide layer (SiO_2), and a silicon oxynitride layer (SiON). However, it is to be understood that the structure can comprise at least one dielectric layer and one or more dielectric layers, which may or may not be arranged in the order described above.

To further this example, the BARC 406 can be, for example, silicon nitride, (SiN), (SRO), silicon oxynitride (*e.g.*, SiO_xN_y, where x and y are selected to provide desired properties) or a silicon rich nitride layer (*e.g.*, SiRN). Alternatively, depending on the optical properties of the materials, the BARC layer 406 can be formed of one or more layers that collectively provide desired antireflective properties. By way of illustration, the following are possible

combinations of materials that could be utilized as the BARC layer 406 in accordance with one or more aspects of the present invention: SiON or SiRN over SiO_2; SiON or SiRN or other antireflective coatings. Using simple organic BARCs (e.g., single layer SiON) is desirable to keep the lithographic process simple. Single layer SiON can be prepared with less difficulty than dual layer SiON, is easier to etch, and is substantially cheaper to utilize. Those skilled in the art will understand and appreciate that various other antireflective materials (*e.g.*, a $SiON/TiO_2$ stack) can also be utilized to form the BARC layer 406 to achieve desired results. For example, the index of refraction of nitride (*e.g.*, Si_3N_4) at light having a wavelength of 630 nm is n=1.9 (k=0). SiON has an index of refraction n=1.73 (k=0) at 630 nm and SiO_2 has an index n=1.43 (k=0) for 630 nm. Additionally, it will be appreciated that the BARC layer 406 can be formed to any suitable thickness to facilitate achieving desired objectives and performance criteria, and that one such suitable thickness for the BARC layer 406 includes a range between about 100 Å to 1500 Å, for example.

The photoresist layer 408 can be, for example, a short wavelength photoresist layer that has been patterned with an image corresponding to a pattern formation utilizing 193 nm or less radiation. An image can be patterned on the photoresist layer 408 utilizing short wavelength radiation, thereby exposing a portion(s) of the layer immediately below the photoresist layer 408. Short wavelength radiation specifically comprises about 193nm light and about 157nm light or less. The image can, for example, correspond to one or more trenches and/or gates. The photoresist layer 408 has pattern lines exhibiting LER 410. Figure 4a also illustrates a distance d1, which is the CD measurement between pairs of resist pattern lines. For purposes of this discussion, d1 represents a desired target CD. This aspect of the invention contemplates a photoresist thickness of between approximately 500 angstroms and approximately 5000 angstroms. For purposes of this particular example, it is not imperative to distinguish between the BARC layer 406 and the dielectric layer 404 in describing photoresist patterning; the example is presented to illustrate that when patterning the photoresist layer 408, resist material is removed to an extent sufficient to expose an immediately inferior layer. Furthermore, to extend this example, many dielectric materials inherently possess anti-reflective properties, (*e.g.*, silicon

oxynitride, ...); thus, a single layer can potentially be substituted to replace the individual dielectric layer(s) 404 and BARC layer 406.

Figure 4b is a top-down illustration of a wafer 400. Resist lines 408 are shown as having been formed utilizing a standard process wherein modern lithographic limits are approached. For example, the lines 408 can be formed *via* utilizing an ArF (153nm) resist. The structures delineated by each pair of resist lines 408 have an associated CD described by the distance d1, where d1 is the target or desired distance between pattern lines. The lines 408 further illustrate LER and/or exposed standing wave(s) associated with typical pattern formation techniques.

It is to be appreciated that the lines 408 can exhibit LER and/or standing wave expression in each of an x-plane, a y-plane and a z-plane (not shown). For example, LER and/or exposed standing wave(s) can exist on a line edge in the y-plane, as illustrated by the cross-sectional view (4a) of the resist lines 408, and/or in the x-plane as shown by the top-down view (4b) of the resist lines 408. It is further to be appreciated that LER and/or standing wave expression can potentially occur in any plane depending on the particular geometry of an object delineated by resist lines.

Figure 5a is an illustration of a wafer as described in Figure 4 undergoing a non-lithographic shrink technique *via* an LER and/or standing wave mitigation system 500. This aspect of the invention contemplates thermal reflow techniques, SAFIER techniques, and/or RELACS™ techniques. However, the invention is not limited to the above-mentioned techniques, and can employ any suitable non-lithographic shrink technique. The LER mitigation system 500 comprises a non-lithographic shrink technique component 502 operably coupled to a monitoring system 504. A processor 506 is operably coupled to a memory 508 and to the monitoring component 504. The processor 506 is associated with an AI component 510 that can make inferences regarding various aspects of LER mitigation.

Still referring to Figure 5, the LER and/or standing wave mitigation system 500 directs the shrink component 502 to perform a shrink technique on a wafer 512. The performance of the technique is illustrated *via* solid arrows. The wafer 512 comprises a silicon or polysilicon substrate 514, at least one layer of dielectric material 516 overlying the substrate 514, a BARC layer 518, and a photoresist

layer 520 overlying the at least one dielectric layer 518. The at least one dielectric layer can be, for example, a silicon carbonitride layer (SiCN), a silicon oxycarbide layer (SiOC:H), a silicon dioxide layer (SiO_2), and a silicon oxynitride layer (SiON). However, it is to be understood that the structure can comprise at least one dielectric layer and one or more dielectric layers, which may or may not be arranged in the order described above. Furthermore, the present invention contemplates utilizing any suitable material for the at least one dielectric layer. As described with respect to Figure 4, the photoresist layer 520 can be, for example, a short wavelength photoresist layer that has been patterned with an image corresponding to a gate formation utilizing 193nm or less radiation. A distance d1 is shown, which is the CD measurement between resist lines. For purposes of this discussion, d1 represents the desired target CD. Furthermore, gate lines exhibiting LER and/or standing wave expression 522 are illustrated as delineating the target CD, as defined by the distance d1.

Figure 5b is a top-down illustration of a wafer with resist lines 522 exhibiting LER and/or exposed standing wave(s). Figure 5b is presented in conjunction with Figure 5a to permit a comparison with the cross-sectional view of the wafer 512 illustrated in Figure 5a in order to facilitate an understanding that the patterned lines 522 can exhibit LER and/or standing wave(s) in one or both of an x-plane and a y-plane. It is further to be appreciated that LER and/or standing wave(s) can also be exhibited in the z-plane or any other plane, depending on the particular geometry of a structure delineated by resist lines.

Figure 6a illustrates a cross-sectional view of a wafer 600 after an LER and/or standing wave mitigation system has performed a non-lithographic shrink technique. The wafer 600 comprises a silicon or polysilicon substrate 602, at least one layer of dielectric material 604 overlying the substrate 602, and a BARC layer 606 interposed between the at least one dielectric layer 604 and a photoresist layer 608. According to this illustration, LER has been mitigated on pattern lines 610. In the process of mitigating LER and/or standing wave(s), it should be noted that the original target CD defined by d1 has been retained.

Figure 6b is a top-down illustration of a wafer having resist lines wherein LER and/or standing wave expression has been mitigated *via* employing a non-lithographic shrink technique. The resist lines 610 further illustrate retention of

target CD, d1. Figure 6b is presented in conjunction with Figure 6a to permit a comparison with the cross-sectional view of the wafer 600 illustrated in Figure 6a.

Figure 7a is a perspective illustration of a resist line 702a on a substrate 704. In describing Figures 7a-d, the word "substrate" is intended to comprise any and/or all of the previously described layers that can comprise a wafer, exclusive of the photoresist layer. As can be seen from the illustration, the resist line 702a exhibits LER 706 in various planes.

Figure 7b is a perspective illustration of a resist line 702b wherein LER has been mitigated *via* employing a non-lithographic shrink technique. The shrink technique is employed utilizing a minimum bake temperature, which can vary from photoresist to photoresist. In this manner, LER can be reduced while CD is preserved within a target tolerance.

Figure 7c is a top-down illustration of a resist line 702c on a substrate 704, the resist lines 702c exhibiting LER 706. Figure 7c is presented in conjunction with Figure 7a to permit a comparison with the perspective view of the resist line 702a illustrated in Figure 7a in order to facilitate an understanding that the resist lines 702 retain a desired CD throughout the process of mitigating LER *via* employing a shrink technique.

Figure 7d is a top-down illustration of a resist line 702d wherein LER has been mitigated *via* employing a non-lithographic shrink technique. The shrink technique is employed utilizing a minimum bake temperature, which can vary depending on the particular type of photoresist being manipulated. In this manner, LER can be reduced while CD is preserved within a target tolerance.

Figure 8a is a cross-sectional illustration of a resist having contact holes 802a on a substrate 804. In describing Figures 8a-d, the word "substrate" is intended to comprise any and/or all of the previously described layers that can comprise a wafer, exclusive of the photoresist layer. The edges of the contact holes 802a exhibit exposed standing waves 806, illustrated as undulate sidewall topography.

Figure 8b is a perspective illustration of a resist having contact holes 802b wherein standing wave expression has been mitigated *via* employing a non-lithographic shrink technique. The shrink technique is employed utilizing a minimum bake temperature. The temperature required to mitigate undesirable topography can vary depending on the type of photoresist. In this manner,

standing wave expression can be reduced while CD is preserved within a target tolerance.

Figure 8c is a top-down illustration of contact holes 802c in a resist overlaying the substrate 804. Figure 8c is presented in conjunction with Figure 8a to permit a comparison with the perspective view of the contact holes 802a illustrated in Figure 8a in order to facilitate an understanding that the contact holes 802 retain a desired CD throughout the process of mitigating standing wave expression *via* employing a shrink technique. Furthermore, Figures 8a and 8c, when viewed in conjunction with one another, illustrate that standing waves can be expressed in either of an x-plane or a y-plane, or both. It is to be appreciated that standing wave expression can occur in any plane, depending on, for example, the particular shape of a structure delineated by patterned lines, the composition(s) of the material(s) employed during wafer fabrication and/or the refractive index thereof, *etc.*

Figure 8d is a top-down illustration of contact holes 802d wherein standing wave expression has been mitigated *via* employing a non-lithographic shrink technique. The shrink technique is employed utilizing a minimum bake temperature as described above. In this manner, standing wave expression can be reduced while CD is maintained within a desired tolerance.

Turning now to Figures 9-11, in accordance with one or more aspects of the present invention, a wafer 902 (or one or more die located thereon) situated on a stage 904 can be logically partitioned into grid blocks to facilitate concurrent measurements of critical dimensions and overlay as the wafer matriculates through a semiconductor fabrication process. This can facilitate selectively determining to what extent, if any, fabrication adjustments are necessary. Obtaining such information can also assist in determining problem areas associated with fabrication processes.

Figure 9 illustrates a perspective view of the steppable stage 904 supporting the wafer 902. The wafer 902 can be divided into a grid pattern as shown in Figure 10. Each grid block (XY) of the grid pattern corresponds to a particular portion of the wafer 902 (*e.g.*, a die or a portion of a die). The grid blocks are individually monitored for fabrication progress by concurrently measuring critical dimensions and overlay with either scatterometry or scanning electron microscope (SEM) techniques.

This can also be applicable in order to assess wafer-to-wafer and lot-to-lot variations. For example, a portion P (not shown) of a first wafer (not shown) can be compared to the corresponding portion P (not shown) of a second wafer. Thus, deviations between wafers and lots can be determined in order to calculate adjustments to the fabrication components that are necessary to accommodate for the wafer-to-wafer and/or lot-to-lot variations.

In Figure 10, one or more respective portions of the wafer 902 (X_1Y_1 ... X_{12}, Y_{12}) are concurrently monitored for critical dimensions and overlay utilizing either scatterometry or scanning electron microscope techniques. Exemplary measurements produced during fabrication for each grid block are illustrated as respective plots. The plots can, for example, be composite valuations of signatures of critical dimensions and overlay. Alternatively, critical dimensions and overlay values can be compared separately to their respective tolerance limits.

As can be seen, the measurement at coordinate X_7Y_6 yields a plot that is substantially higher than the measurement of the other portions XY. This can be indicative of overlay, overlay error, and/or one or more critical dimension(s) outside of acceptable tolerances. As such, fabrication components and/or operating parameters associated therewith can be adjusted accordingly to mitigate repetition of this aberrational measurement. It is to be appreciated that the wafer 902 and or one or more die located thereon can be mapped into any suitable number and/or arrangement of grid blocks to effect desired monitoring and control.

Figure 11 is a representative table of concurrently measured critical dimensions and overlay taken at various portions of the wafer 902 mapped to respective grid blocks. The measurements in the table can, for example, be amalgams of respective critical dimension and overlay signatures. As can be seen, all the grid blocks, except grid block X_7Y_6, have measurement values corresponding to an acceptable value (V_A) (*e.g.*, no overlay error is indicated and/or overlay measurements and critical dimensions are within acceptable tolerances), while grid block X_7Y_6 has an undesired value (V_U) (*e.g.*, overlay and critical dimensions are not within acceptable tolerances, thus at least an overlay or CD error exists). Thus, it has been determined that an undesirable fabrication condition exists at the portion of the wafer 902 mapped by grid block X_7Y_6. Accordingly, fabrication process components and parameters can be adjusted as

described herein to adapt the fabrication process accordingly to mitigate the re-occurrence or exaggeration of this unacceptable condition.

Alternatively, a sufficient number of grid blocks can have desirable thickness measurements so that the single offensive grid block does not warrant scrapping the entire wafer. It is to be appreciated that fabrication process parameters can be adapted so as to maintain, increase, decrease and/or qualitatively change the fabrication of the respective portions of the wafer 902 as desired. For example, when the fabrication process has reached a pre-determined threshold level (*e.g.*, X% of grid blocks have acceptable CDs and no overlay error exists), a fabrication step can be terminated.

Turning briefly to Figures 12, 13, and 14, methodologies that can be implemented in accordance with the present invention are illustrated. While, for purposes of simplicity of explanation, the methodologies are shown and described as a series of blocks, it is to be understood and appreciated that the present invention is not limited by the order of the blocks, as some blocks can, in accordance with the present invention, occur in different orders and/or concurrently with other blocks from that shown and described herein. Moreover, not all illustrated blocks may be required to implement the methodologies in accordance with the present invention.

Figure 12 is an illustration of a methodology 1200 in accordance with an aspect of the present invention. Utilizing conventional methods, resist lines are formed in a resist layer on a semiconductor substrate at 1202. It is to be appreciated that the lines can delineate, for example, trenches, gates, or any other suitable structure that can be patterned onto or into a photoresist. The formation of lines conforms to a specific target tolerance with regard to a critical dimension. At 1204, the present system makes a determination of the existence of LER and/or standing wave expression on the lines. This determination can be made *via* employing, for example, a monitoring component such as a scanning electron microscope (SEM), a critical dimension SEM (CD-SEM), a scatterometry component, or any other suitable means for detecting, measuring, and/or monitoring LER and/or standing wave expression. If no LER and/or standing wave expression is detected, the method can proceed directly to 1212, where pattern line structure is approved. If LER is detected, a non-lithographic shrink technique can be employed to mitigate LER and/or standing wave expression at

1206. The non-lithographic shrink technique can be, for example, a thermal reflow technique, a Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS^{TM}) technique, and/or a Shrink Assist Film for Enhanced Resolution (SAFIER) technique. At 1208, a determination is made regarding whether LER and/or standing wave expression has been mitigated. If the undesired topography associated therewith has not been successfully mitigated, then the methodology reverts to 1206, where a non-lithographic shrink technique can be performed again. If topographical mitigation is determined to have been successful at 1208, the methodology proceeds to 1210, where a determination is made regarding whether an original target CD has been retained. If the specified target tolerance for CD has not been achieved, then the method proceeds to 1214, where resist lines are rejected. If the CD measured at 1210 is within a tolerance associated with a target CD value, then the method proceeds to 1212, where pattern lines are approved.

Figure 13 illustrates a flow diagram of a methodology 1300 in accordance with an aspect of the invention. At 1302, lines are formed in a resist *via* a conventional lithographic technique(s). At 1304, a determination is made regarding whether LER and/or standing wave(s) are present. If no LER and/or standing wave(s) are detected, the lines are approved at 1312. If LER and/or standing wave(s) are detected on the lines, a thermal flow technique can be employed at 1306 to mitigate any undesirable topography. At 1308, an inquiry is made regarding whether LER and/or standing wave(s) have been successfully mitigated. If not, the methodology returns to 1308 for another attempt. If the unwanted topography has been successfully mitigated, the methodology can proceed to 1310, where an inquiry is made as to whether post-mitigation CD is within a tolerance associated with a target CD. If the post-mitigation CD is not within a desired tolerance, the method permits the rejection of the patterned lines at 1314. If the target CD tolerance is satisfied at 1310, the lines can be approved at 1312.

Figure 14 is an illustration of a flow diagram of a methodology in accordance with an aspect of the present invention. Resist lines are formed in a photoresist *via* a conventional lithographic technique(s) at 1402. At 1404, a determination is made as to whether LER and/or standing wave(s) are present. If no LER and/or standing wave(s) are detected, the lines can be approved at 1414.

If LER and/or standing wave(s) are detected on the lines, the method employs artificial intelligence (AI) techniques at 1406 to infer, for example, a suitable duration for employing a non-lithographic shrink technique at 1408 to mitigate LER and/or standing wave(s). According to another example, AI techniques can be employed to determine a most-suitable non-lithographic shrink technique, such as thermal reflow, RELACS™, SAFIER, *etc.* At 1410, an inquiry is made regarding whether LER and/or standing wave(s) have been successfully mitigated. If not, the methodology returns to 1408 for another attempt. If it is determined that the unwanted topography has been successfully mitigated, the methodology can proceed to 1412, where an inquiry is made as to whether post-mitigation CD is within a tolerance associated with a target CD. If the post-mitigation CD is not within a desired tolerance, the method permits the rejection of the patterned lines at 1416. If the target CD tolerance is satisfied at 1412, the lines can be approved at 1414.

Figure 15 is a schematic block diagram of an exemplary operating environment for a system configured in accordance with the present invention. In order to provide additional context for various aspects of the present invention, Figure 15 and the following discussion are intended to provide a brief, general description of a suitable computing environment 1510 in which the various aspects of the present invention can be implemented. While the invention has been described above in the general context of computer-executable instructions that can run on one or more computers, those skilled in the art will recognize that the invention also can be implemented in combination with other program modules and/or as a combination of hardware and software. Generally, program modules comprise routines, programs, components, data structures, *etc.*, that perform particular tasks or implement particular abstract data types. Moreover, those skilled in the art will appreciate that the inventive methods can be practiced with other computer system configurations, including single-processor or multiprocessor computer systems, minicomputers, mainframe computers, as well as personal computers, hand-held computing devices, microprocessor-based or programmable consumer electronics, and the like, each of which can be operatively coupled to one or more associated devices. The illustrated aspects of the invention can also be practiced in distributed computing environments where certain tasks are performed by remote processing devices that are linked through a

communications network. In a distributed computing environment, program modules can be located in both local and remote memory storage devices.

With reference to Figure 15, an exemplary environment 1510 for implementing various aspects of the invention comprises a computer 1512, the computer 1512 including a processing unit 1514, a system memory 1516 and a system bus 1518. The system bus 1518 couples system components including, but not limited to, the system memory 1516 to the processing unit 1514. The processing unit 1514 can be any of various commercially available processors. Dual microprocessors and other multi-processor architectures also can be employed as the processing unit 1514.

The system bus 1518 can be any of several types of bus structure including a memory bus or memory controller, a peripheral bus and a local bus utilizing any of a variety of commercially available bus architectures. The system memory 1522 comprises read only memory (ROM) 1520 and random access memory (RAM) 1522. A basic input/output system (BIOS), containing the basic routines that help to transfer information between elements within the computer 1512, such as during start-up, is stored in ROM 1520.

The computer 1512 further comprises a hard disk drive 1524, a magnetic disk drive 1526, (*e.g.*, to read from or write to a removable disk 1528) and an optical disk drive 1530, (*e.g.*, for reading a CD-ROM disk 1532 or to read from or write to other optical media). The hard disk drive 1524, magnetic disk drive 1526 and optical disk drive 1530 can be connected to the system bus 1518 by a hard disk drive interface 1534, a magnetic disk drive interface 1536 and an optical drive interface 1538, respectively. The drives and their associated computer-readable media provide nonvolatile storage of data, data structures, computer-executable instructions, *etc.* for the computer 1512, including for the storage of broadcast programming in a suitable digital format. Although the description of computer-readable media above refers to a hard disk, a removable magnetic disk and a CD, it should be appreciated by those skilled in the art that other types of media which are readable by a computer, such as zip drives, magnetic cassettes, flash memory cards, digital video disks, cartridges, and the like, can also be used in the exemplary operating environment, and further that any such media can contain computer-executable instructions for performing the methods of the present invention.

A number of program modules can be stored in the drives and RAM 1522, including an operating system 1540, one or more application programs 1542, other program modules 1544 and program data 1546. It is to be appreciated that the present invention can be implemented with various commercially available operating systems or combinations of operating systems.

A user can enter commands and information into the computer 1512 through a keyboard 1548 and a pointing device, such as a mouse 1550. Other input devices (not shown) can comprise a microphone, an IR remote control, a joystick, a game pad, a satellite dish, cameras, in the sense of gesture interpreted through cameras and machine-vision software, a scanner, or the like. These and other input devices are often connected to the processing unit 1514 through a serial port interface 1552 that is coupled to the system bus 1518, but can be connected by other interfaces, such as a parallel port, a game port, a universal serial bus ("USB"), an IR interface, *etc.* A monitor 1554 or other type of display device is also connected to the system bus 1518 *via* an interface, such as a video adapter 1556. In addition to the monitor, a computer typically comprises other peripheral output devices (not shown), such as speakers, printers *etc.*

The computer 1512 can operate in a networked environment utilizing logical connections to one or more remote computers, such as a remote computer(s) 1558. The remote computer(s) 1558 can be a workstation, a server computer, a router, a personal computer, microprocessor based entertainment appliance, a peer device or other common network node, and typically comprises many or all of the elements described relative to the computer 1512, although, for purposes of brevity, only a memory storage device 1560 is illustrated. The logical connections depicted comprise a local area network (LAN) 1562 and a wide area network (WAN) 1564. Such networking environments are commonplace in offices, enterprise-wide computer networks, intranets and the Internet.

When used in a LAN networking environment, the computer 1512 is connected to the local network 1562 through a network interface or adapter 1566. When used in a WAN networking environment, the computer 1512 typically comprises a modem 1568, or is connected to a communications server on the LAN, or has other means for establishing communications over the WAN 1564, such as the Internet. The modem 1568, which can be internal or external, is

connected to the system bus 1518 *via* the serial port interface 1552. In a networked environment, program modules depicted relative to the computer 1512, or portions thereof, can be stored in the remote memory storage device 1560. It will be appreciated that the network connections shown are exemplary and other means of establishing a communications link between the computers can be used.

What has been described above comprises examples of the present invention. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the present invention, but one of ordinary skill in the art can recognize that many further combinations and permutations of the present invention are possible. Accordingly, the present invention is intended to embrace all such alterations, modifications and variations that fall within the spirit and scope of the appended claims. Furthermore, to the extent that the term "comprises" is used in either the detailed description or the claims, such term is intended to be inclusive in a manner similar to the term "comprising" as "comprising" is interpreted when employed as a transitional word in a claim.